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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,884	07/15/2003	Michael Maldei	INTECH 3.0-083	7447

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,884	MALDEI ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *16-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 5, 8, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Sung et al. (US/5,814,862).

The rejection that was mailed on June 15, 2004 is maintained and repeated herein below as of record.

Re claim 1, Sung et al. disclose a method of fabricating a semiconductor device, comprising: patterning a mask (31) on a surface of a semiconductor wafer to expose portions of the semiconductor wafer while covering other portions of the semiconductor wafer (see Fig. 2G); etching selected portions of the semiconductor wafer to form a plurality of recesses (22') between gate contacts (50) disposed in a first region of the semiconductor wafer (see Figs. 2G, 2H, 3A and 3B); depositing a conductive layer (40 40') to fill the recesses (22') and to cover the gate contacts (50) (see Fig. 2I); and depositing a metal layer (44) (see Fig. 2K), wherein the metal layer (44) contacts at least a portion of the conductive layer (40) and is in electrical contact with the conductive layer filling the recess (see Figs. 2F – 3B; Col. 4, line 65 – Col. 7, line 21).

Re claim 2, as applied to claim 1 above, Sung et al. disclose all the claimed limitations including the limitation depositing an insulating layer (42) over the conductive layer prior to depositing the metal layer (see Fig. 2J); patterning a bitline mask (43) on the insulating layer;

and etching selected portions of the insulating layer in accordance with the bitline mask to form a trench through the insulating layer to contact the conductive layer (see Fig. 2K), wherein the metal layer (42) is deposited in the trench (42') (see Figs. 2F – 3B; Col. 4, line 65 – Col. 7, line 21).

Re claim 5, as applied to claim 1 above, Sung et al. disclose all the claimed limitations including the limitation wherein the insulating layer (42) is an oxide (see Col. 6, lines 49-61).

Re claim 8, as applied to claim 1 above, Sung et al. disclose all the claimed limitations including the limitation wherein the metal layer (44) comprises a refractory metal (see Col. 7, lines 11-13).

Re claim 15, as applied to claim 1 above, Sung et al. disclose all the claimed limitations including the limitation wherein the conductive layer (40) comprises tungsten (see Col. 6, line 16-25).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. (US/5,814,862) in view of Cote et al. (US/6,236,079).

The rejection that was mailed on June 15, 2004 is maintained and repeated herein below as of record.

Re claims 3 and 4, as applied in claim 2 in Paragraph 2 above, Sung et al. teach all the claimed limitations including etching of the selected portions of the insulating layer (42) that includes over-etching through the insulating layer (42) to ensure exposure of the conductive layer (40) and the conductive layer (40) covers top surfaces of the gate contacts (50) (see Fig. 2K).

However, Sung et al. do not specifically disclose the using conventional reactive ion etching (RIE) process.

Cote et al. discloses method of via-etching for metallization process the method includes using RIE to etch the insulating layer (see Fig. 4 and 7). As Cote et al. disclose, RIE process is used in order to from vias having vertical sidewall.

Both Sung et al. and Cote et al. teachings are directed to method of fabricating semiconductor device the method includes forming vias to form an interconnect in the semiconductor device. Therefore, the teachings of Sung et al. and Cote et al. are analogous.

One of ordinary skill in the art would have been motivated to use RIE process during etching of the insulating layer in order to from vias having vertical sidewall.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Sung et al. reference RIE process during etching of the insulating layer as taught by Cote et al. in order to from vias having vertical sidewall.

5. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. (US/5,814,862) in view of Wolf et al., (Silicon Processing for The VLSI Era, Volume 1: Process Technology, Pp. 184, (1986)).

The rejection that was mailed on June 15, 2004 is maintained and repeated herein below as of record.

Re claims 6 and 7, as applied in claim 5 in Paragraph 2 above, Sung et al. disclose all the claimed limitations including forming of an oxide layer.

However, Sung et al. do not specifically disclose use of TOES precursor to form the oxide layer having a thickness least 1000 Å thick.

Wolf et al. disclose forming of silicon oxide by LPCVD process using TOES precursor. Wolf et al. disclose that TEOS films generally show excellent conformality (see Wolf et al. Page 184).

Both Sung et al. and Wolf et al. teachings are directed to method of fabricating semiconductor device the method includes forming dielectric layer during fabrication of semiconductor device. Therefore, the teachings of Sung et al. and Wolf et al. are analogous.

One of ordinary skill in the art would have been motivated to use TEOS precursor in order to form conformal silicon oxide film.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Sung et al. reference with TEOS precursor to form an oxide layer as taught by Wolf et al. in order to form conformal silicon oxide film.

Furthermore, the claimed thickness would have been formed within the level of ordinary skill in the art by routine optimization in order to achieve the desired device size and performance.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed thickness range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable

recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. (US/5,814,862) in view of Nitayama et al. (US/6,236,079).

The rejection that was mailed on June 15, 2004 is maintained and repeated herein below as of record.

Re claim 9, as applied in clam 8 in Paragraph 2 above, Sung et al. disclose all the claimed limitations including forming the refractory metal.

However, Sung et al. do not disclose the refractory metal is being tungsten.

Nitayama et al. disclose method of forming a semiconductor device the method includes depositing of tungsten metal (W) (102) (see Fig. 5I) to fill the recess in contact with the portion of conductive poly-Si layer (106). As shown in Fig. 5I, Nitayama et al. disclose that tungsten (W) (102) formed in conductively contact with the poly-Si layer in order to form the bit-line.

Both Sung et al. and Nitayama et al. teachings are directed to method of fabricating semiconductor device the method includes forming vias to form an interconnect and filling the vias with conductive layer. Therefore, the teachings of Sung et al. and Nitayama et al. are analogous.

One of ordinary skill in the art would have been motivated to form a refractory conductive metal comprises tungsten as alternative material in order to connect the bit-line to the bit-line contact.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Sung et al. reference with a refractory

conductive metal comprises tungsten as taught by Nitayama et al. in order form the bit-line and connect the bit-line to the bit-line contact.

7. Claims 10, 11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. (US/5,814,862) in view of Parekh et al. (US/6,383,868).

The rejection that was mailed on June 15, 2004 is maintained and repeated herein below as of record.

Re clams 10, 11, and 14, as applied to claim 1 in Paragraph 2 above, Sung et al. disclose all the claimed limitations including forming of a conductive layer (plug).

However, Sung et al. do not specifically disclose the conventional conductive material of silicon that comprises poly-silicon to form plug and doping the silicon plug.

Parekh et al. discloses forming doped polysilicon conductive layer (51) in the contact holes (50) in order to form self aligned contact plug (see Parekh et al. Fig. 1, Col. 4, lines 37-64).

Both Sung et al. and Parekh et al. teachings are directed to method of fabricating semiconductor device the method includes forming vias to form an interconnect and filling the vias with conductive layer to from conductive plug. Therefore, the teachings of Sung et al. and Parekh et al. are analogous.

One of ordinary skill in the art would have motivated to form doped conductive silicon layer in the contact holes in order to form self aligned contact plug.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Sung et al. reference with doped silicon conductive material such as doped polysilicon as taught by Parekh et al. in order to form self aligned contact plug.

8. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. (US/5,814,862) and Parekh et al. (US/6,383,868), as applied to claim 10 in Paragraph 11 above, and further in view of Taniguchi et al. (US/6,690,050).

Re claims 12 and 13, as applied to claim 10 in Paragraph 7 above, Sung et al. and Parekh et al. in combination disclose all the claimed limitations including forming of a conductive layer (plug) comprising silicon (polysilicon).

However, Sung et al. and Parekh et al. do not specifically disclose the conventional conductive material of silicon that comprises amorphous silicon and annealing of the amorphous silicon.

Taniguchi et al. disclose method of fabricating memory cell the method comprises forming of conductive silicon plug of amorphous silicon (31) and annealing of the amorphous silicon to convert the amorphous silicon to polysilicon (see Taniguchi et al. Fig. 7; Col. 6, line 48 – Col. 9, line 59; Col. 25, lines 44-52).

Sung et al., Parekh et al., and Taniguchi et al. teachings are directed to method of fabricating semiconductor device the method includes forming vias to form an interconnect and filling the vias with conductive layer to from conductive plug. Therefore, the teachings of Sung et al., Parekh et al., and Taniguchi et al. are analogous.

One of ordinary skill in the art would have been motivated to form an amorphous silicon and anneal the amorphous silicon in order to form polysilicon contact plug.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Sung et al. and Parekh et al. reference

with form an amorphous silicon and anneal the amorphous silicon as taught by Taniguchi et al. in order to form self aligned polysilicon contact plug.

Response to Arguments

9. Applicants' arguments filed on September 16, 2004 have been fully considered but they are not persuasive.

Applicants argue that "There is no teaching or suggestion in *Sung* to deposit a conductive layer to cover the gate contacts, including keeping the gat contacts covered by the layer even during subsequent process..."

In response to applicants' argument, it is respectfully submitted Sung et al. '862 disclose all the claimed limitations as applied above. Sung et al. '862 disclose blanket deposition of the conductive layer 40 over the structure including over the gate contacts prior etching back of the conductive layer (see Sung et al. '862, Col. 6, lines 16-Col. 44). In the absence specific process step in the claim, blanket deposition of the conductive layer 40 over the structure including over the gate contacts prior etching back of the conductive layer meets the claim limitation of claim 1, i.e., *depositing a conductive layer to fill the recess and to cover the gate contacts*.

In addition, claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

In response to applicants' argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *keeping the*

gat contacts covered by the layer even during subsequent process) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Further in response to applicants' with respect to claims 2, 5, 8, and 15, it is respectfully submitted that claims 2, 5, 8, and 15 are not allowable because the base independent claim, i.e., claim 1, is not allowable.

Therefore, the rejection of claims 1, 2, 5, 8, and 15 under 35 U.S.C. 102 is deemed proper.

In response to applicants' argument with respect to claims rejection of claims 3 and 4 under 35 U.S.C. 103, it is respectfully submitted that the combination of Sung et al. '862 and Cote et al. '079 disclose all the claimed limitations as set forth herein above and claims 3 and 4 are not allowable because the base claims, i.e., claims 1 and 2, are not allowable.

In response to applicants' argument with respect to claims rejection of claims 6 and 7 under 35 U.S.C. 103, it is respectfully submitted that the combination of Sung et al. '862 and Wolf et al. disclose all the claimed limitations as set forth herein above and claims 6 and 7 are not allowable because the base claims, i.e., claims 1 and 5, are not allowable.

In response to applicants' argument with respect to claims rejection of claim 9 under 35 U.S.C. 103, it is respectfully submitted that the combination of Sung et al. '862 and Nitayama et al. '097 disclose all the claimed limitation as set forth herein above and claim 9 is not allowable because the base claims, i.e., claims 1 and 8, are not allowable.

In response to applicants' argument with respect to claims rejection of claims 10, 11, 14 under 35 U.S.C. 103, it is respectfully submitted that the combination of Sung et al. '862 Parekh et al. '868 disclose all the claimed limitations as set forth herein above and claims 10, 11, and 14 are not allowable because the base claim, i.e., claims 1, is not allowable.

In response to applicants' argument with respect to claims rejection of claims 12 and 13 under 35 U.S.C. 103, it is respectfully submitted that the combination of Sung et al. '862, Parekh et al. '868, and Taniguchi et al. '050 disclose all the claimed limitations as set forth herein above and claims 12 and 13 are not allowable because the base claim, i.e., claim 1, is not allowable.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
November 22, 2004

George Fourson
Primary Examiner